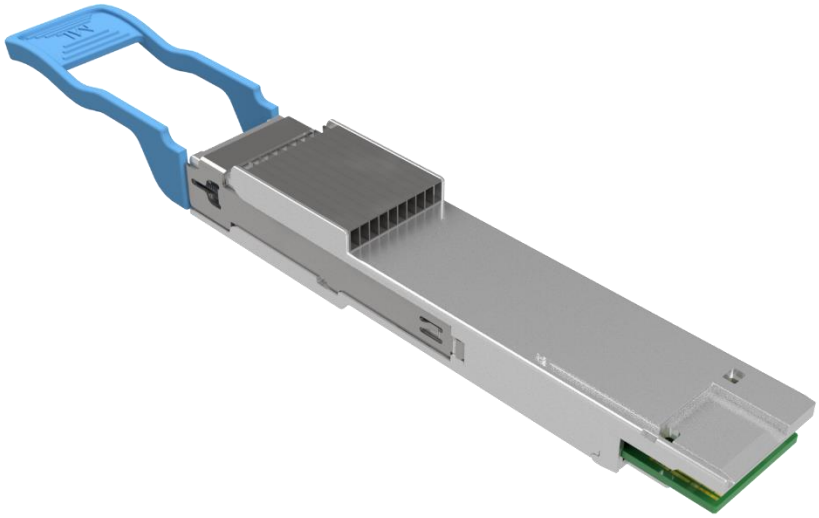
ML4062-LB2a-6dB
ML4062-LB2a-9dB

Technical Reference

QSFP-DD Electrical Passive Loopback Module
Loss Target Loopbacks
CMIS 4.0 Compliant



Innovation for the next generation

Table of Contents

ML4062-LB2a-6dB/9dB QSFP-DD Passive Loopback Module – Key Features

- ✓ QSFP-DD MSA Form Factor
- ✓ Supports 8x112G electrical interface
- ✓ Loops back TX to RX on all 8 ports
- ✓ Built with advanced PCB material
- ✓ Loss Target Loopbacks with 6 and 9 dB attenuation at 26 GHz to emulate specific DAC loss profiles
- ✓ Programmable MSA memory pages
- ✓ I2C Interface
- ✓ Separate daughter card for power spots
- ✓ 4 independent power heaters, dissipating up to 30W
- ✓ 4 temperature sensors
- ✓ Voltage Sense
- ✓ 2 status LED Indicator
- ✓ Insertions counter
- ✓ Cut-off temperature preventing module overheating
- ✓ Hot Pluggable module
- ✓ Type 2A module with heat sink height 3.4 mm

LED Indicator

Green (Solid) – Signifies that the module is operating in high power mode.
Red (Solid) – Signifies the module is operating in low power mode.
Green (Blinking) – Module in high power mode and Voltage or Temperature Alarm is triggered.
Red (Blinking) – Module in Low power mode and Voltage or Temperature Alarm is triggered.

Operating Conditions

Parameter	Symbol	Notes/Conditions	Min	Typ	Max	Units
Operating Temperature	T_A		-40	-	+105	°C
Supply Voltage	VCC	Main Supply Voltage	3.00	3.3	3.6	V
Input/output Load Resistance	RL	AC-Coupled, Differential	90	100	110	Ω
Power Class		Programmable to Emulate all power classes	0	-	30	W
Bit Rate		56G NRZ 112G PAM4			112	Gbps

1. General Description

ML4062-LB2a-6dB/9dB is used for testing QSFP-DD transceiver ports under board level tests, by substituting a full-featured QSFP-DD transceiver with the **ML4062-LB2a-6dB/9dB**. The **ML4062-LB2a-6dB/9dB** covers all QSFP-DD power classes.

The **ML4062-LB2a-6dB/9dB** is packaged in a standard MSA housing compatible with all QSFP-DD ports. It provides an economical way to exercise QSFP-DD ports during R&D validation, production testing, and field testing.

Note that the **ML4062-LB2a-6dB/9dB** follows the **CMIS Rev 4.0** standard.

2. Functional Description

2.1 Management Data Interface – I2C

The **ML4062-LB2a-6dB/9dB** supports the I2C interface.

2.2 I2C Signals, Addressing and Frame Structure

2.2.1 I2C Frame

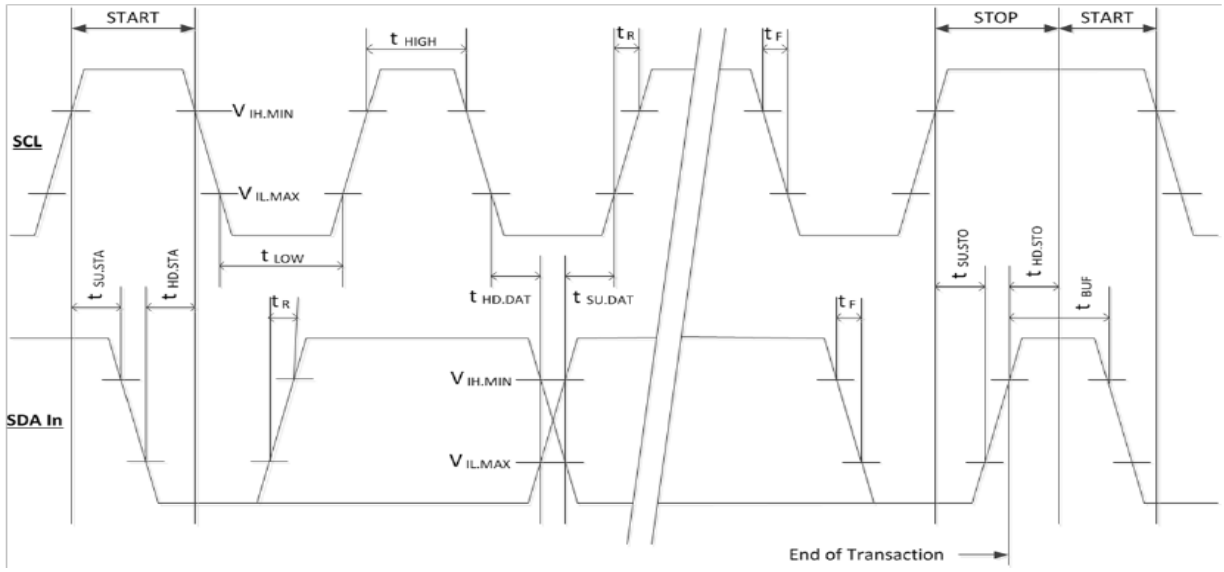


Figure 1: QSFP-DD Timing Diagram

Before initiating a 2-wire serial bus communication, the host will provide setup time on the ModSelL line of all modules on the 2-wire bus. The host will not change the ModSelL line of any module until the 2-wire serial bus communication is complete and the hold time requirement is satisfied. The 2-wire serial interface address of the QSFP-DD module is 1010000X (A0h).

In order to allow access to multiple QSFP-DD modules on the same 2-wire serial bus, the QSFP-DD pin-out includes a module select pin (ModSelL). This pin (which is pulled high in the module) must be held low by the host to select the module of interest and allow communication over the 2-wire serial interface. The module do not respond to or accept 2-wire serial bus instructions unless it is selected.

2.2.2 Management Timing Parameters

The timing parameters for the 2-Wire interface to the QSFP-DD module are shown in the table below:

Parameter	Symbol	Min	Max	Unit
Clock Frequency	fSCL	0	400	KHz
Clock Pulse Width Low	tLOW	1.3		us
Clock Pulse Width High	tHigh	0.6		us
Time bus free before new transmission can start	tBUF	20		us
START Hold Time	tHD.STA	0.6		us
START Set-up Time	tSU.STA	0.6		us
Data In Hold Time	tHD.DAT	0		us
Data in Setup Time	tSU.DAT	0.1		us
Input Rise Time (400kHz)	tR.400		300	ns
Input Fall Time (400kHz)	tF.400		300	ns
STOP Setup Time	tSU.STO	0.6		us
ModSelL Setup Time	tSU.ModSelL	2		ms
ModSelL Hold Time	tHD.ModSelL	2		ms
Aborted sequence – bus release	Deselect_Abort	2		ms

2.2.3 Memory Specifications

QSFP-DD memory transaction timings are given in the following table:

Parameter	Symbol	Min	Typ	Max	Unit
Serial Interface Clock Holdoff "Clock Stretching"	T_clock_hold			500	us
Complete Single Write	tWR			5	ms
Endurance (Write Cycles)		50K			cycles

2.2.4 Device Addressing and Operation

Clock and Data Transitions: The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods indicate a START or STOP condition. All addresses and data words are serially transmitted to and from the QSFP-DD in 8-bit words.
Every Byte on the SDA line must be 8-bits long. Data is transferred with the most significant bit (MSB) first.

START Condition: A high-to-low transition of SDA with SCL high is a START condition, which must precede any other command.

STOP Condition: A low-to-high transition of SDA with SCL high is a STOP condition.

Acknowledge: After sending each 8-bit word, the transmitter releases the SDA line for one bit time, during which the receiver is allowed to pull SDA low (zero) to acknowledge (ACK) that it has received each word.

Memory (Management Interface) Reset: After an interruption in protocol, power loss or system reset the QSFP-DD Module management interface can be reset. Memory reset is intended only to reset the QSFP-DD transceiver management interface (to correct a hung bus). No other module functionality is implied.

1. Clock up to 9 cycles
2. Look for SDA high in each cycle while SCL is high
3. Create a Start condition as SDA is high

Device Addressing: QSFP-DD devices require an 8-bit device address word following a start condition to enable a read or write operation. The device address word consists of a mandatory sequence for the first seven most significant bits in Figure 2. This is common to all QSFP-DD devices.

1	0	1	0	0	0	0	R/W
MSB							LSB

Figure 2: QSFP-DD Device Address

The eighth bit of the device address is the read/write operating select bit. A read operation is initiated if this bit is set high and a write operation is initiated if this bit is set low. Upon compare of the device address (with ModSelL in the low state) the QSFP-DD Module will output a zero (ACK) on the SDA line to acknowledge the address.

2.3 QSFP-DD Memory Map

2.3.1 Full Map

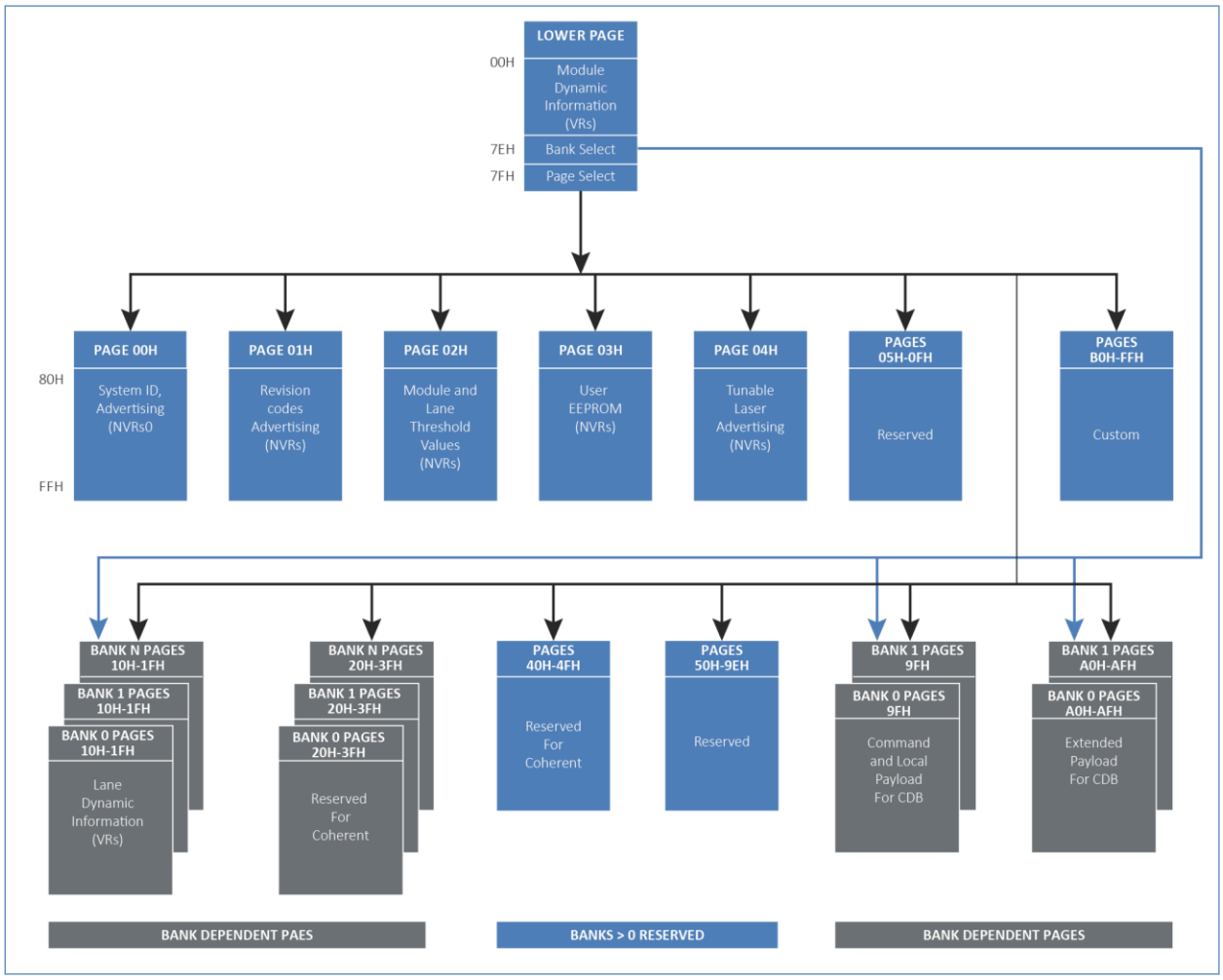


Figure 3: QSFP-DD Memory Map

This section defines the Memory Map for QSFP-DD transceiver used for serial ID, digital monitoring and certain control functions. The interface is mandatory for all QSFP-DD devices.
The structure of the memory is shown in Figure 3. The memory space is arranged into a lower, single page, address space of 128 bytes and multiple upper address space pages. This structure permits timely access to addresses in the lower page, e.g. Interrupt Flags and Monitors. Less time critical entries, e.g. serial ID information and threshold settings are available with the Page Select function. The structure also provides address expansion by adding additional upper pages as needed.

2.3.2 ML4062-LB2a-6dB/9dB Memory Map

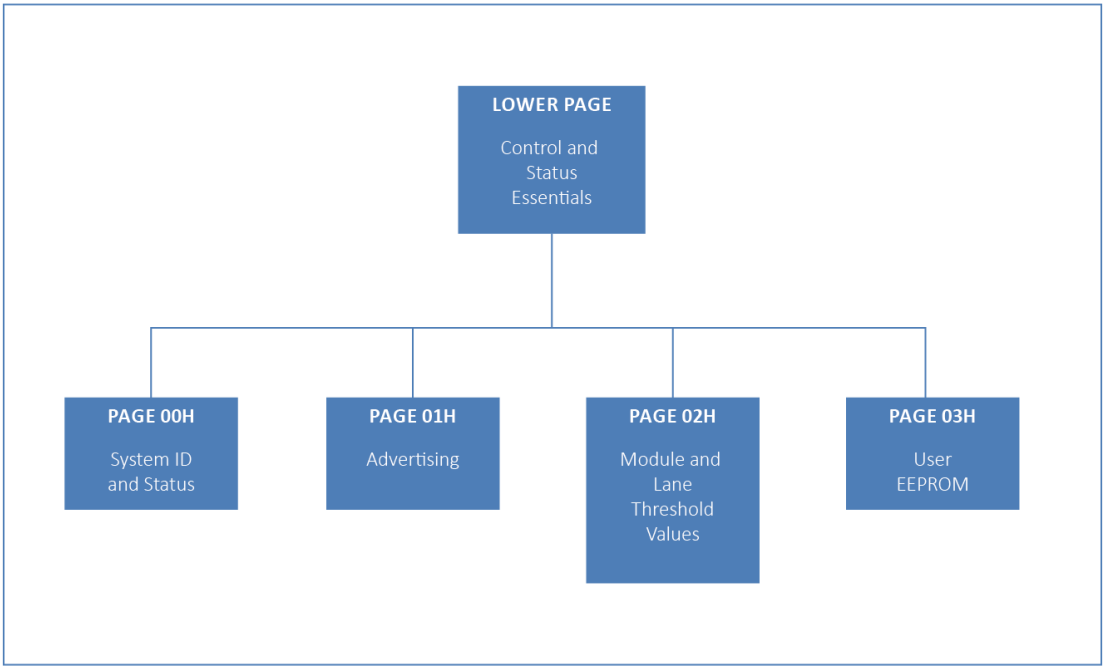


Figure 4: Implemented Memory Map

2.3.3 Memory Accessibility

The Memory Map registers types are shown in the table below:

Page Address	Address Range	Type
Lower Page	0-25	RO
	26	RW (VR)
	27-126	RO
	127	RW (VR)
Page 00h	128-165	RO
	166-181	RW (NVR)
	182-255	RO
Page 01h	128-255	RO
Page 02h	128-255	RO
Page 03 Lower Page	128-131	RW (NVR)
	132-133	RO
	134-138	RW (NVR)
	139	RW
	140-151	RW (NVR)
	152-159	RO
	160-255	RW (NVR)
	0-25	RO
	26	RW (VR)

2.3.4 Memory Content

The table below shows the memory content.

Address	Hex	Decimal	ASCII	MSA Description
LowMem 0(00h)	0x18	24		Identifier
LowMem 1(01h)	0x40	64	@	Revision Compliance
LowMem 2(02h)	0x00	0		Flat-mem / TWI Max Speed
LowMem 3(03h)	0x00	0		Module State / Software interrupt
LowMem 4(04h)	0x00	0		Bank 0 flag summary
LowMem 5(05h)	0x00	0		Bank 1 flag summary
LowMem 6(06h)	0x00	0		Bank 2 flag summary
LowMem 7(07h)	0x00	0		Bank 3 flag summary
LowMem 8(08h)	0x00	0		Data Path/Module FW fault and Module State changed flag
LowMem 9(09h)	0x00	0		Latched VCC3.3/Temp Alarm and Warning
LowMem 10(0Ah)	0x00	0		Latched AUX1/2 Alarm and Warning
LowMem 11(0Bh)	0x00	0		Latched Vendor Defined/AUX3 Alarm and Warning
LowMem 12(0Ch)	0x00	0		Reserved
LowMem 13(0Dh)	0x00	0		Custom
LowMem 14(0Eh)				Internally measured Temperature T.S.3 MSB
LowMem 15(0Fh)				Internally measured Temperature T.S.3 LSB
LowMem 16(10h)				Internally measured Supply VCC net MSB
LowMem 17(11h)				Internally measured Supply VCC net LSB
LowMem 18-21 (12h-15h)	0x00	0		
LowMem 22(16h)				Internally measured Supply VCCRx net MSB
LowMem 23(17h)				Internally measured Supply VCCRx net LSB
LowMem 24(18h)				Internally measured Temperature T.S.1 MSB
LowMem 25(19h)				Internally measured Temperature T.S.1 LSB
LowMem 26(1Ah)	0x40	64		Software reset / Low power control
LowMem 27-38 (1Bh-26h)	0x00	0		
LowMem 39(27h)	0x01	1		Major FW Rev
LowMem 40(28h)	0x00	0		Minor FW Rev

LowMem 41-125 (29h-7Dh)	0x00	0		
LowMem 126(7Eh)	0x00	0		Bank Select Byte
LowMem 127(7Fh)	0x00	0		Page Select Byte
Page00 128(80h)	0x18	24		Identifier
Page00 129(81h)	0x4D	77	M	Vendor Name
Page00 130(82h)	0x55	85	U	Vendor Name
Page00 131(83h)	0x4C	76	L	Vendor Name
Page00 132(84h)	0x54	84	T	Vendor Name
Page00 133(85h)	0x49	73	I	Vendor Name
Page00 134(86h)	0x4C	76	L	Vendor Name
Page00 135(87h)	0x41	65	A	Vendor Name
Page00 136(88h)	0x4E	78	N	Vendor Name
Page00 137(89h)	0x45	69	E	Vendor Name
Page00 138(8Ah)	0x20	32		Vendor Name
Page00 139(8Bh)	0x20	32		Vendor Name
Page00 140(8Ch)	0x20	32		Vendor Name
Page00 141(8Dh)	0x20	32		Vendor Name
Page00 142(8Eh)	0x20	32		Vendor Name
Page00 143(8Fh)	0x20	32		Vendor Name
Page00 144(90h)	0x20	32		Vendor Name
Page00 145(91h)	0x00	0		Vendor OUI
Page00 146(92h)	0x00	0		Vendor OUI
Page00 147(93h)	0x00	0		Vendor OUI
Page00 148(94h)	0x4D	77	M	Vendor PN
Page00 149(95h)	0x4C	76	L	Vendor PN
Page00 150(96h)	0x34	52	4	Vendor PN
Page00 151(97h)	0x30	48	0	Vendor PN
Page00 152(98h)	0x36	54	6	Vendor PN
Page00 153(99h)	0x32	50	2	Vendor PN
Page00 154(9Ah)	0x2D	45	-	Vendor PN

Page00 155(9Bh)	0x4C	76	L	Vendor PN
Page00 156(9Ch)	0x42	66	B	Vendor PN
Page00 157(9Dh)	0x32	50	2	Vendor PN
Page00 158(9Eh)	0x61	97	a	Vendor PN
Page00 159(9Fh)	0x2D	45	-	Vendor PN
Page00 160(A0h)	0x36	54	6	Vendor PN
Page00 161(A1h)	0x64	100	d	Vendor PN
Page00 162(A2h)	0x42	66	B	Vendor PN
Page00 163(A3h)	0x20	32		Vendor PN
Page00 164(A4h)	0x20	32		Vendor Rev
Page00 165(A5h)	0x20	32		Vendor Rev
Page00 166(A6h)	0x20	32		Vendor SN
Page00 167(A7h)	0x20	32		Vendor SN
Page00 168(A8h)	0x20	32		Vendor SN
Page00 169(A9h)	0x20	32		Vendor SN
Page00 170(AAh)	0x20	32		Vendor SN
Page00 171(ABh)	0x20	32		Vendor SN
Page00 172(ACh)	0x20	32		Vendor SN
Page00 173(ADh)	0x20	32		Vendor SN
Page00 174(AEh)	0x20	32		Vendor SN
Page00 175(AFh)	0x20	32		Vendor SN
Page00 176(B0h)	0x20	32		Vendor SN
Page00 177(B1h)	0x02	32		Vendor SN
Page00 178(B2h)	0x20	32		Vendor SN
Page00 179(B3h)	0x20	32		Vendor SN
Page00 180(B4h)	0x20	32		Vendor SN
Page00 181(B5h)	0x20	32		Vendor SN
Page00 182(B6h)	0x31	49	1	Date Code
Page00 183(B7h)	0x39	57	9	Date Code
Page00 184(B8h)	0x30	48	0	Date Code

Page00 185(B9h)	0x39	57	9	Date Code
Page00 186(BAh)	0x31	49	1	Date Code
Page00 187(BBh)	0x37	55	7	Date Code
Page00 188(BCh)	0x30	48	0	Date Code
Page00 189(BDh)	0x31	49	1	Date Code
Page00 190(BEh)	0x00	0		CLEI Code
Page00 191(BFh)	0x00	0		CLEI Code
Page00 192(C0h)	0x00	0		CLEI Code
Page00 193(C1h)	0x00	0		CLEI Code
Page00 194(C2h)	0x00	0		CLEI Code
Page00 195(C3h)	0x00	0		CLEI Code
Page00 196(C4h)	0x00	0		CLEI Code
Page00 197(C5h)	0x00	0		CLEI Code
Page00 198(C6h)	0x00	0		CLEI Code
Page00 199(C7h)	0x00	0		CLEI Code
Page00 200(C8h)	0xE0	224	?	Module Power Characteristics
Page00 201(C9h)	0x5D	93	]	Module Power Characteristics
Page00 202(CAh)	0x00	0		Cable assembly length
Page00 203(CBh)	0x00	0		Media Connector Type
Page00 204(CCh)	0x01	1		Copper Cable Attenuation
Page00 205(CDh)	0x01	1		Copper Cable Attenuation
Page00 206(CEh)	0x02	2		Copper Cable Attenuation
Page00 207(CFh)	0x03	3		Copper Cable Attenuation
Page00 208(D0h)	0x00	0		Copper Cable Attenuation
Page00 209(D1h)	0x00	0		Copper Cable Attenuation
Page00 210(D2h)	0x00	0		Cable Assembly Lane Information
Page00 211(D3h)	0x00	0		Cable Assembly Lane Information
Page00 212(D4h)	0x00	0		Media Interface Technology
Page00 213-220 (D5h-DCh)	0x00	0		
Page00 222(DEh)				Checksum

Page00 223-255 (DFh-FFh)	0x00	0		Custom Info NV
Page01 128(80h)	0x00	0		Inactive Major FW Rev
Page01 129(81h)	0x00	0		Inactive Minor FW Rev
Page01 130(82h)	0x01	1		Module Major HW Rev
Page01 131(83h)	0x01	1		Module Minor HW Rev
Page01 132(84h)	0x00	0		link length SMF
Page01 133(85h)	0x00	0		link length (OM5)
Page01 134(86h)	0x00	0		link length (OM4)
Page01 135(87h)	0x00	0		link length (OM3 50um)
Page01 136(88h)	0x00	0		link length (OM2 50um)
Page01 137(89h)	0x00	0		Reserved
Page01 138(8Ah)	0x00	0		Nominal Wavelength
Page01 139(8Bh)	0x00	0		Nominal Wavelength
Page01 140(8Ch)	0x00	0		Wavelength Tolerance
Page01 141(8Dh)	0x00	0		Wavelength Tolerance
Page01 142(8Eh)	0x04	4		Implemented Management Interface features advertising
Page01 143(8Fh)	0xDF	223	?	Implemented Management Interface features advertising
Page01 144(90h)	0x00	0		Implemented Management Interface features advertising
Page01 145(91h)	0x04	4		Module Characteristics advertising
Page01 146(92h)	0x55	85	U	Module Characteristics advertising
Page01 147(93h)	0xD8	216	?	Module Characteristics advertising
Page01 148(94h)	0x00	0		Module Characteristics advertising
Page01 149(95h)	0x00	0		Module Characteristics advertising
Page01 150(96h)	0x91	145	?	Module Characteristics advertising
Page01 151(97h)	0x00	0		Module Characteristics advertising
Page01 152(98h)	0x00	0		Module Characteristics advertising
Page01 153(99h)	0x00	0		Module Characteristics advertising
Page01 154(9Ah)	0x00	0		Module Characteristics advertising
Page01 155(9Bh)	0x00	0		Implemented Controls advertising
Page01 156(9Ch)	0x00	0		Implemented Controls advertising

Page01 157(9Dh)	0x00	0		Implemented Flags advertising
Page01 158(9Eh)	0x00	0		Implemented Flags advertising
Page01 159(9Fh)	0x33	51	3	Implemented Monitors advertising
Page01 160(A0h)	0x00	0		Implemented Monitors advertising
Page01 161(A1h)	0x00	0		Implemented Signal Integrity Controls advertising
Page01 162(A2h)	0x00	0		Implemented Signal Integrity Controls advertising
Page01 163-254 (A3h-FEh)	0x00	0		
Page01 255(FFh)	0xDA	218		Checksum
Page02 128(80h)	0x50	80		Temperature monitor high alarm threshold MSB
Page02 129(81h)	0x00	0		Temperature monitor high alarm threshold LSB
Page02 130(82h)	0x00	0		Temperature monitor low alarm threshold MSB
Page02 131(83h)	0x00	0		Temperature monitor low alarm threshold LSB
Page02 132(84h)	0x4b	75		Temperature monitor high warning threshold MSB
Page02 133(85h)	0x00	0		Temperature monitor high warning threshold LSB
Page02 134(86h)	0x05	5		Temperature monitor low warning threshold MSB
Page02 135(87h)	0x00	0		Temperature monitor low warning threshold LSB
Page02 136(88h)	0x8C	140		Supply 3.3-volt monitor high alarm threshold MSB
Page02 137(89h)	0xA0	160		Supply 3.3-volt monitor high alarm threshold LSB
Page02 138(8Ah)	0x75	117		Supply 3.3-volt monitor low alarm threshold MSB
Page02 139(8Bh)	0x30	48		Supply 3.3-volt monitor low alarm threshold LSB
Page02 140(8Ch)	0x8A	138		Supply 3.3-volt monitor high warning threshold MSB
Page02 141(8Dh)	0xAC	172		Supply 3.3-volt monitor high warning threshold LSB
Page02 142(8Eh)	0x77	119		Supply 3.3-volt monitor low warning threshold MSB
Page02 143(8Fh)	0x24	36		Supply 3.3-volt monitor low warning threshold LSB
Page02 144-254 (90h-FEh)	0x00	0		
Page02 255(FFh)	0x42	66		Checksum
Page03 129-131 (81h-83h)	0x00	0		User EEPROM
Page03 132(84h)				Insertion Counter MSB
Page03 133(85h)				Insertion Counter LSB
Page03 134(86h)	0x55	85		Cut-Off temperature

Page03 135(87h)				PWM controller 1
Page03 136(88h)				PWM controller 2
Page03 137(89h)				PWM controller 3
Page03 138(8Ah)				PWM controller 4
Page03 139(8Bh)				LPMode/ModSelL State/Edge Detection
Page03 140(8Ch)				IntL Control Register
Page03 141(8Dh)				static Controller 5
Page03 142(8Eh)	0x00	0		User EEPROM NVR
Page03 143(8Fh)	0x00	0		User EEPROM NVR
Page03 144(90h)	0x00	0		User EEPROM NVR
Page03 145(91h)	0x00	0		User EEPROM NVR
Page03 146(92h)	0x00	0		User EEPROM NVR
Page03 147(93h)	0x00	0		User EEPROM NVR
Page03 148(94h)	0x00	0		User EEPROM NVR
Page03 149(95h)	0x00	0		User EEPROM NVR
Page03 150(96h)	0x00	0		User EEPROM NVR
Page03 151(97h)	0x00	0		User EEPROM NVR
Page03 152(98h)				Internally measured Temperature T.S.2 MSB
Page03 153(99h)				Internally measured Temperature T.S.2 LSB
Page03 154(9Ah)				Internally measured Temperature T.S.4 MSB
Page03 155(9Bh)				Internally measured Temperature T.S.4 LSB
Page03 156(9Ch)				Copy of VCC MSB
Page03 157(9Dh)				Copy of VCC LSB
Page03 158(9Eh)				Internally measured Supply VCCTx net MSB
Page03 159(9Fh)				Internally measured Supply VCCTx net LSB
Page03 160-254 (A0h-FEh)	0x00	0		User EEPROM NVR

2.4 Low Speed Electrical Hardware Pins

In addition to the 2-wire serial interface the module has the following low speed pins for control and status:

- ModselL
- ResetL
- LPMode
- IntL
- ModPrstL

2.4.1 ModselL

The ModSelL is an input signal to the module that is pulled up to Vcc in the QSFP-DD module. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple QSFP-DD modules on a single 2-wire interface bus. When ModSelL is “High”, the module will not respond to or acknowledge any 2-wire interface communication from the host.

2.4.2 ResetL

ResetL, is an active-low signal, and must be asserted for longer than the minimum reset pulse duration to trigger a module reset.

2.4.3 LPMode

LPMode is an input signal to the module from the host, operating with active high logic. The LPMode signal is pulled up to Vcc in the QSFP-DD module through 4.75 KOhm resistor. The LPMode signal intervenes in the Module State Transition (refer to section 2.5.2 for more details).

2.4.4 IntL

IntL is an output signal. When the IntL signal is asserted Low it indicates a change in module state, a possible module operational fault or a status critical to the host system. The IntL signal is deasserted “High” after all set interrupt flags are read.

2.4.5 ModPrstL

ModPrsL is grounded in the module. The ModPrsL is asserted “Low” when the module is inserted and deasserted “High” when the module is physically absent from the host connector.

2.5 ML4062-LB2a-6dB/9dB Specific Functions

2.5.1 Module State

The Module State describes module-wide behaviors and properties. The **ML4062-LB2a-6dB/9dB** implements two module states: ModuleLowPwr and ModuleReady.
The ModuleLowPwr state is a host control state, where the management interface is fully initialized and operational and the Module is in Low Power mode, where the Power Spots are deactivated. During this state, the host may configure the module using the management interface and memory map. The module state encoding for ModuleLowPwr is 001.
The ModuleReady state is a host control state that indicates that the module is in High Power mode, and the PWM is activated. The module state encoding for ModuleReady is 011.

Address	Bit	Name	Description	Type
3 (lower Page)	3~1	Module State	Current state of Module: 001b= ModuleLowPwr 011b= ModuleReady	RO

2.5.2 Module State Transition

The state transition between Low Power and High Power is related to three parameters:
1. ForceLowPwr bit– software control (forces module into low power mode), register 26 bit 4
2. LowPwr bit – software control, register 26 bit 6
3. LPMode – Hardware signal

According to these parameters, the state of the module is defined. Conditions for Low Power and High Power state, are summarized in the table below.

ForceLowPwr (Reg 26 bit 4)	LowPwr (register 26 bit 6)	LPMode	State
1	X	X	Low Power
0	1	1	Low Power
0	1	0	High Power
0	0	1	High Power
0	0	0	High Power

2.5.3 Module Global Controls

Module global controls are control aspects that are applicable to the entire module on all channels in the module.

Address	Bit	Name	Description	Type
26(lower Page)	6	LowPwr	Parameter used to control the module power mode (refer to section 2.5.2) Default value =1	RW
	4	ForceLowPwr	0b = high power mode(default) 1b =Forces module into low power mode	
	3	Software Reset	Self-clearing bit that causes the module to be reset. The effect is the same as asserting the reset pin for	

			the appropriate hold time, followed by its de-assertion. This bit will be cleared to zero on a reset so a value of 0 will always be returned. 0b = not in reset 1b = Software reset	
3(lower page)	0	Software Interrupt	Digital state of Interrupt: 0b = Interrupt source is present 1b = No interrupt source present	RO

2.5.4 Status Register

Register 141 of page 03 reports the digital state of the QSFP-DD low speed signals.

Address	Bit	Name	Description	Type
141 (Page 03)	0	ModSel	Digital state of ModSel pin	RO
	1	LPMode	Digital state of LPMode	

Note that when the ModSelL is High the I2C will stop working and the user will read FF from register 141.

2.5.5 Digital State Detection

The module must be able to detect the digital state of the LPMode and ModSelL signals. An I2C latch register in upper page 03 is latched on both rising and falling edges of the LPMode and ModSelL signals.

Address	Bit	Name	Description	Type
141 (Page 03)	4	ModSelL transection	Read 0b: No edge detected Read 1b: Either rising or falling edges detected Write 0b: No effect Write 1b: Clear the register	RW
	5	LPMode transection		

2.5.6 Digital Control of IntL

During power-up of the module, IntL is defaulted to negated. Afterward, host can set the status of this signal to any status through register 142 in upper page 03.

Address	Bit	Name	Description	Type
142 (Page 03)	1	IntL control	0xb: Normal operation 10b: Force IntL to logic 0, VIntL < Vol(max) 11b: Force IntL to logic 1, VIntL > Voh(min)	RW (NVR)
	0			

2.5.7 Temperature Monitor

The **ML4062-LB2a-6dB/9dB** has 4 internal temperature sensors, on the PCBA, in order to continuously monitor the module's temperature. Internally measured Module temperature are represented as a 16-bit signed two's complement value in increments of 1/256 degrees Celsius, yielding a total range of –127 °C to +128 °C that is considered valid between –40 °C and +125 °C.

Address	Bit	Name	Description	Type
14 (lower Page)	ALL	Temperature MSB	Internally measured module temperature 4 (shell T.S)	RO
15 (lower Page)	ALL	Temperature LSB	Internally measured module temperature 4 (shell T.S)	
150 Page 3	ALL	Custom Temperature MSB	Internally measured temperature 1 (PCB Bottom)	
151 Page 3	ALL	Custom Temperature LSB	Internally measured temperature 1 (PCB Bottom)	
152 Page 3	ALL	Temperature MSB	Internally measured temperature 2 (PCB Bottom)	
153 Page 3	ALL	Temperature LSB	Internally measured temperature 2 (PCB Bottom)	
154 Page 3	ALL	Temperature MSB	Internally measured temperature 3 (PCB Top)	
155 Page 3	ALL	Temperature LSB	Internally measured temperature 3 (PCB Top)	

The distribution of internal temperature sensors is shown in the figure 5.

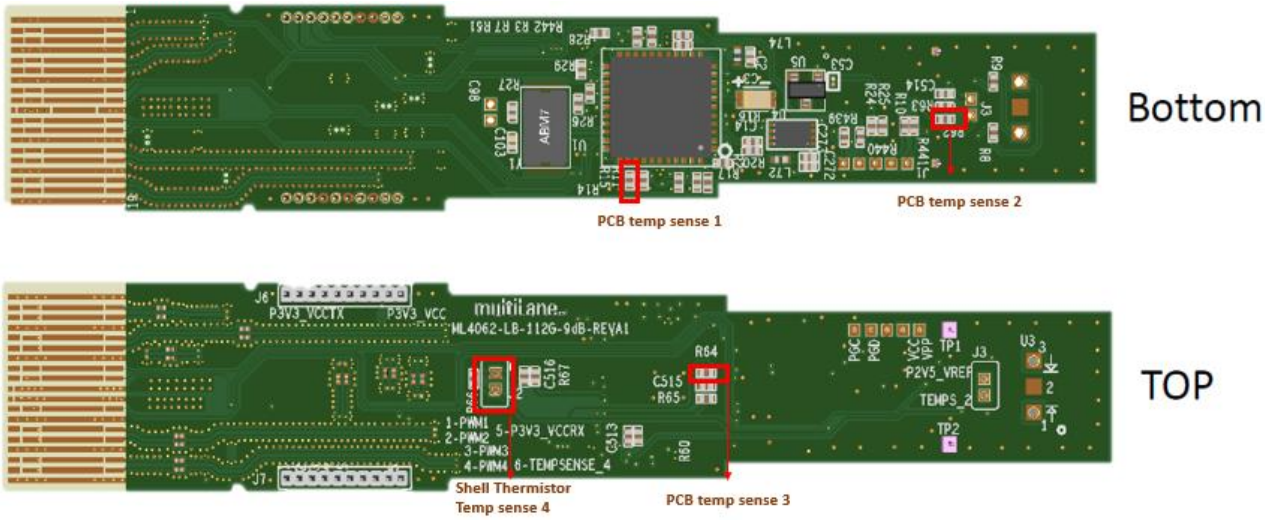


Figure 5: temperature sensor location

The temperature Alarms and warnings interrupt flags exists in lower page.

Address	Bit	Name	Description	Type
9 (lower Page)	3	L-Temp Low Warning	Latched low temperature warning flag	RO
	2	L-Temp High Warning	Latched high temperature warning flag	
	1	L-Temp Low Alarm	Latched low temperature alarm flag	
	0	L-Temp High Alarm	Latched high temperature alarm flag	

Note that any interrupt flag when asserted will generate the interrupt. Its state is read from register 3 bit 0.

2.5.8 Voltage Sense

Three voltage sense circuits are available in the **ML4062-LB2a-6dB/9dB** that allow to measure the internal supplied voltage on each power net, with LSB unit is 0.1 mV.

Address	Bit	Name	Description	Type
16	All	Supply voltage MSB	Internally measured supply voltage VCC Net	RO
17	All	Supply voltage LSB		
22	All	Supply voltage MSB	Internally measured supply voltage VCCRX Net	
23	All	Supply voltage LSB		
158	All	Supply voltage MSB	Internally measured supply voltage VCCTX Net	
159	All	Supply voltage LSB		

The Voltage Alarms and warnings interrupt flags exists in lower page.

Address	Bit	Name	Description	Type
9 (lower Page)	7	L-Vcc3.3v Low Warning	Latched low 3.3 volts supply voltage warning flag	RO
	6	L-Vcc3.3v High Warning	Latched low 3.3 volts supply voltage warning flag	
	5	L-Vcc3.3v Low Alarm	Latched low 3.3 volts supply voltage alarm flag	
	4	L-Vcc3.3v High Alarm	Latched low 3.3 volts supply voltage alarm flag	

2.5.9 Programmable Power Dissipation and Thermal Emulation

The power spots are distributed on a separate board, a daughter card that is mounted on the PCBA, which contains only the power spots.
The daughter card contains four thermal spots that are heated relative to the related control registers settings. The distribution of these spots is shown in the image below (Figure6).

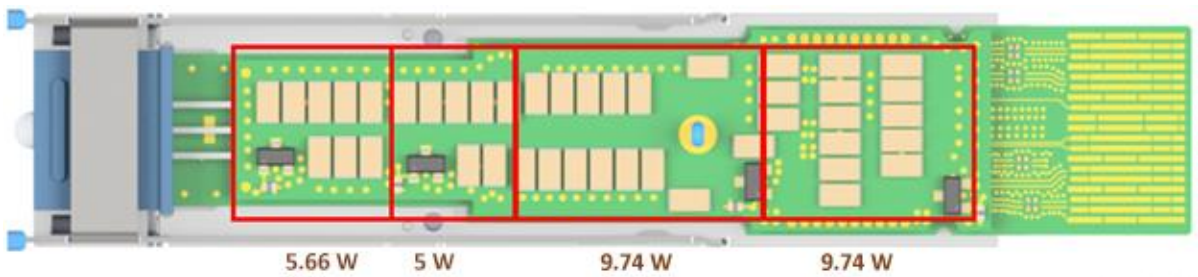


Figure 6: Thermal spots distribution

Registers described in the table below are used to control thermal spots over I2C. They are 8 bits data wide registers.

The consumed power changes accordingly when the values of these registers are changed (only in high power mode). In Low power mode the module automatically turns off all power spots. The values written in these registers are permanently stored.

Address	Bit	Name	Description	Type
135 Page 03	7:0	PWM controller 1	9.74W top power spot PWM control register (net P3V3_VccRx)	RO
136 Page 03	7:0	PWM controller 2	9.74W top power spot PWM control register (net P3V3_Vcc)	
137 Page 03	7:0	PWM controller 3	5W bottom power spot PWM control register (net P3V3_VccTx)	
138 Page 03	7:0	PWM controller 4	5.66W bottom power spot PWM control register (net P3V3_VccTx)	

Figure7 shows a side view of the distribution of thermal pads. The grey shapes at the top of the daughter card are TIM for heat conduction to the shell. The TIM conductivity is 3 W/m.K.

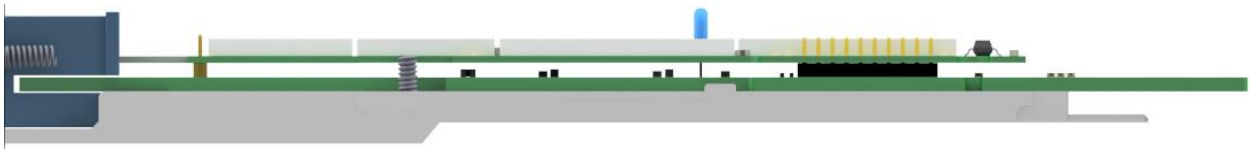


Figure 7: Module side view

2.5.10 Cut-Off Temperature

To avoid overheating the module, a Cut-Off Temperature is pre-defined.
The module is continuously monitoring the temperature and checking its value against the Cut-Off temperature. Once the module temperature reaches the cut-off temperature, all power spots will automatically turn off in order to prevent overheating. Once the temperature is 5 degrees below cut-off value, previous values are reloaded to all control registers.
The maximum Cut-Off temperature for the **ML4062-LB2a-6dB/9dB** is 100 ˚C and it can be programmed to any value from register 134 of memory page 3. Its default value is 100 ˚C.

Address	Bit	Name	Description	Type
134	7:0	Cut-Off temperature	Module Cut-Off Temperature, LSB = 1 degC	RW (NVR)

2.5.11 Insertion counter

The Insertion counter contains the number of times the module was plugged in a host. The insertion counter is incremented every time the module goes in initializing sequence, as it is nonvolatile it is always saved. The insertion counter can be read from registers 132-133 page03.

Address	Bit	Name	Description	Type
132 (page 03)	MSB	Insertion Counter MSB		RO
133 (page 03)	LSB	Insertion Counter LSB	LSB unit = 1 insertion	

2.5.12 Alarm and Warning Thresholds

Each monitoring variable has a corresponding high alarm, low alarm, high warning and low warning thresholds. These factory preset values allow the user to determine when a particular value is exceeding the predefined limit. While Voltage LSB unit is 100 µV and Temperature LSB unit is 1/256 ˚C. Note that these addresses are of memory Page 02.

Address	Bit	Name	Default Value	Type
128(Page 02)	ALL	high temp alarm threshold (MSB)	95 °C	RO
129(Page 02)	ALL	high temp alarm threshold (LSB)		
130(Page 02)	ALL	low temp alarm threshold (MSB)	0 °C	
131(Page 02)	ALL	low temp alarm threshold (LSB)		
132(Page 02)	ALL	high temp warning threshold (MSB)	85 °C	
133(Page 02)	ALL	high temp warning threshold (LSB)		
134(Page 02)	ALL	low temp warning threshold (MSB)	5 °C	
135(Page 02)	ALL	low temp warning threshold (LSB)		
136(Page 02)	ALL	high volt alarm threshold (MSB)	3.6 V	
137(Page 02)	ALL	high volt alarm threshold (LSB)		
138(Page 02)	ALL	low volt alarm threshold (MSB)	3.0 V	
139(Page 02)	ALL	low volt alarm threshold (LSB)		
140(Page 02)	ALL	high volt warning threshold (MSB)	3.55 V	
141(Page 02)	ALL	high volt warning threshold (LSB)		
142(Page 02)	ALL	low volt warning threshold (MSB)	3.05 V	
143(Page 02)	ALL	low volt warning threshold (LSB)		

2.5.13 FW and HW Revision

Information about the FW and HW revision are present in Lower Page, registers 39-40, and in Page01 registers 130-131, respectively, as described in the table below.

Address	Bit	Description	Type
39 (Lower Page)	All	Major FW Rev	RO
40 (Lower Page)	All	Minor FW Rev	
130 (page 01)	All	Major HW Rev	
131 (page 01)	All	Minor HW Rev	

3. High Speed Signals

High speed signals are electrically looped back from TX side to RX side of the module, all differential TX pairs are connected to the corresponding RX pairs, and the signals are AC coupled as specified by QSFP-DD MSA High Speed Electrical specifications.

3.1 ML4062-LB2a-6dB Insertion Loss graph

The Passive traces connecting TX to RX pairs result in a 6dB attenuation on the high-speed signals in the ML4062-LB2a-6dB.
The graph below shows the insertion loss data of the ML4062-LB2a-6dB, for all eight channels.

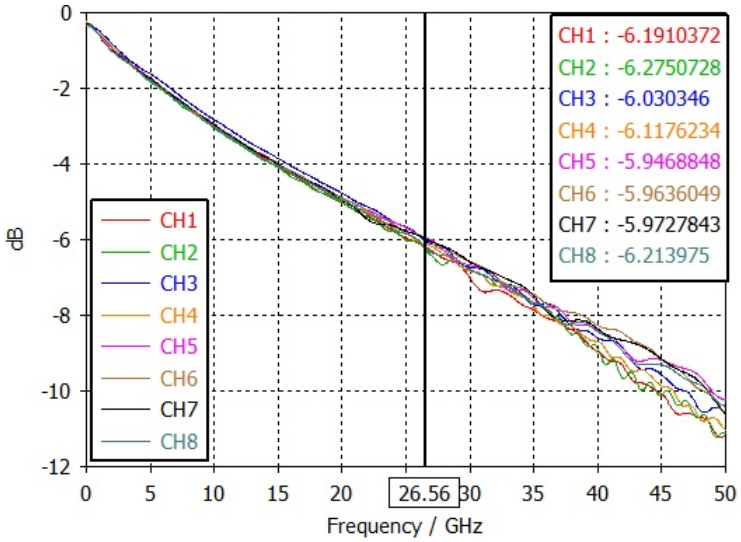


Figure 8: -6dB Insertion Loss

3.2 ML4062-LB2a-9dB Insertion Loss graph

The Passive traces connecting TX to RX pairs result in a 9 dB attenuation on the high-speed signals in the ML4062-LB2a-9dB.
The graph below shows the insertion loss simulated data of the ML4062-LB2a-9dB, for all eight channels.

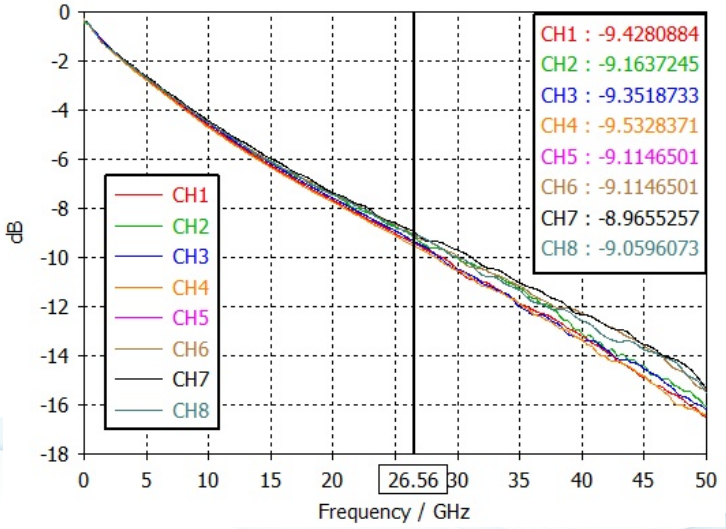


Figure 9: -9dB Insertion Loss

4. QSFP-DD Pin Allocation

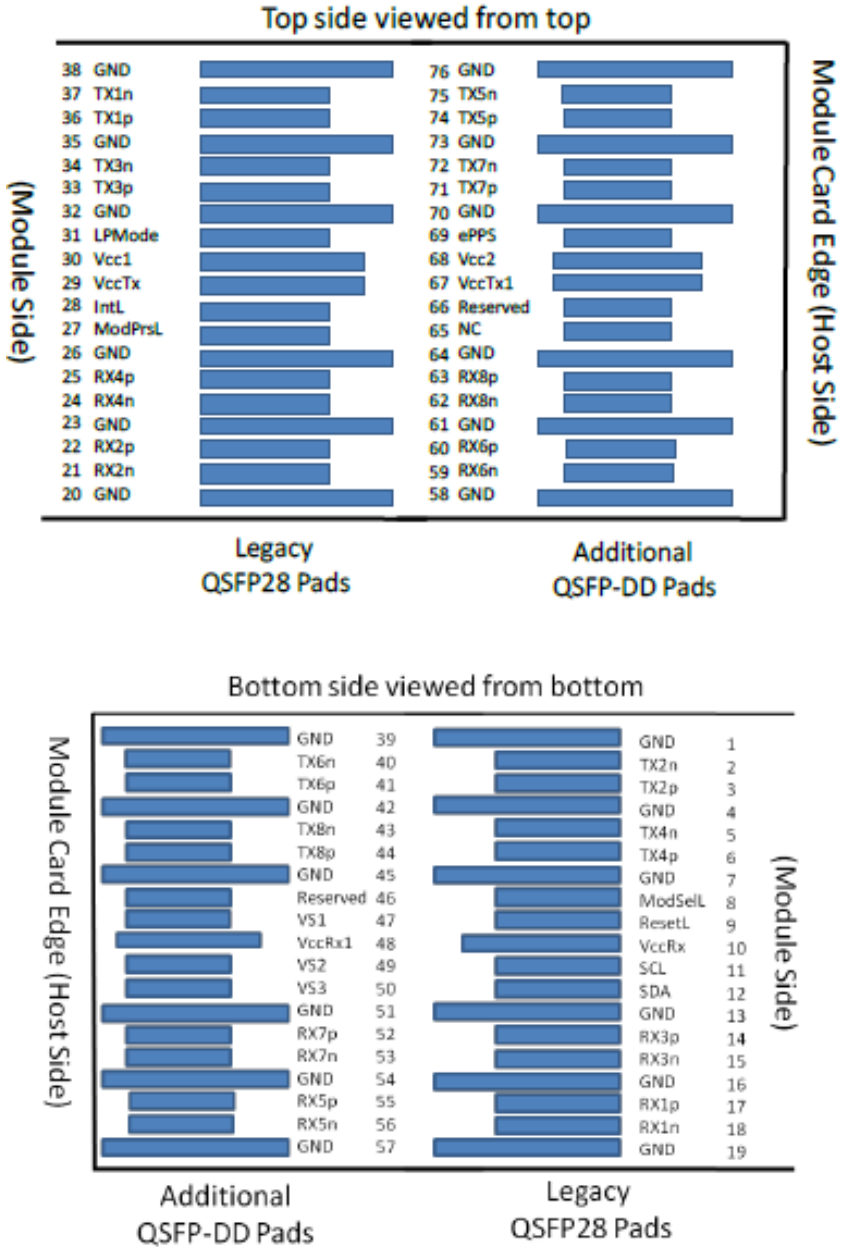


Figure 10: QSFP-DD Module Pad Layout

5. Mechanical Dimensions

A general description of mechanical dimensions of the **ML4062-LB2a-6dB/9dB** is shown in the image below.

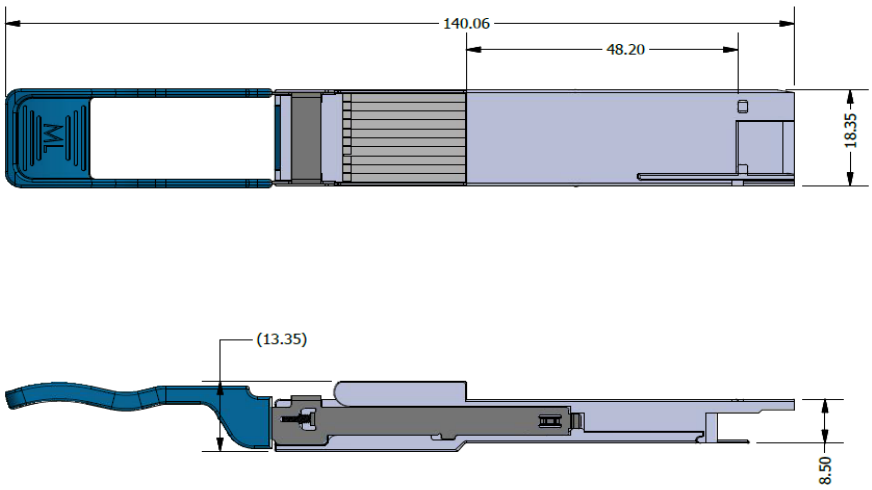


Figure 11: Mechanical Dimensions

Revision History

Revision number	Date	Description
0.1	6/24/2021	▪ Preliminary
0.2	9/20/2021	▪ Update operating temperature range ▪ Update section 2.5.4: Status register ▪ Update section 2.5.5: Digital State Detection register ▪ Update section 2.5.6: Digital Control of IntL register ▪ Update section 2.5.10: cut-off temperature ▪ Update section 2.5.12: temperature alarm/warning thresholds
0.21	10/7/2021	▪ Text and format updates

multiLane

multiLane

North America
48521 Warm Springs Blvd. Suite 310
Fremont, CA 94539
USA
+1 510 573 6388

Worldwide
Houmal Technology Park
Askarieh Main Road
Houmal, Lebanon
+961 81 794 455

Asia
14F-5/ Rm.5, 14F., No 295
Sec.2, Guangfu Rd. East Dist.,
Hsinchu City 300, Taiwan (R.O.C)
+886 3 5744 591